

MM5298 8192-Bit (8192 x 1) Dynamic RAM**

General Description

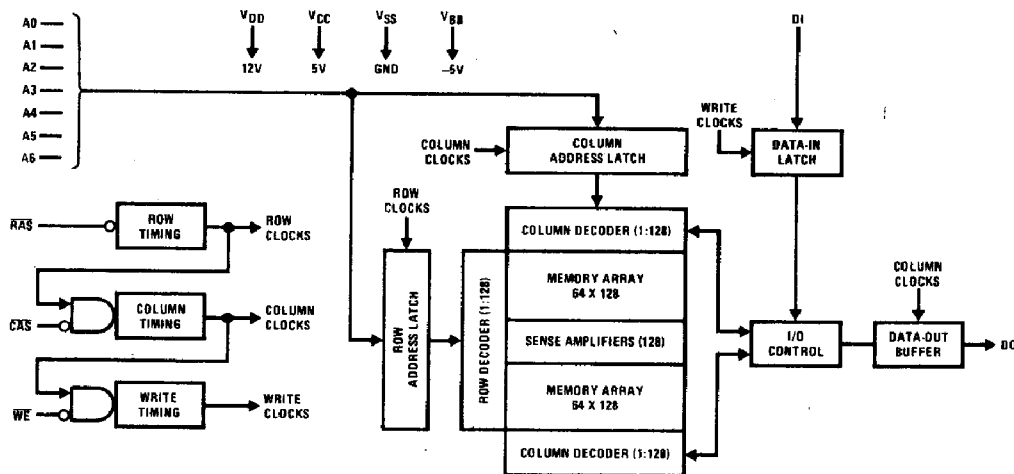
The MM5298 is an 8192 x 1-bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5298 to be used in page mode operation. The MM5298 employs the same masks and highly reliable production-proven 2-layer polysilicon NMOS technology as the MM5290.

As shown in the block diagram, the MM5298 is available as either the upper or lower half of the MM5290. Address A5 selects the operating half. For MM5298A, A5 should be low (V_{IL}) during row address hold time (t_{RAH}). For MM5298B, A5 should be high (V_{IH}) during t_{RAH} . The MM5298 requires only 64 cycles of Refresh every 2 ms. This can be accomplished by performing any cycle which brings the RAS active including an RAS-only cycle at each of the 64 row addresses used.

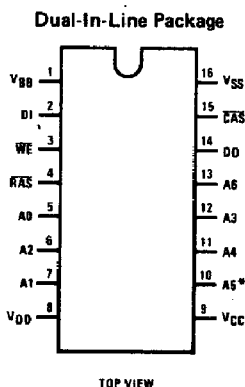
Features

- 100% DC and AC compatible with MM5290
- Only 64 Refresh cycles every 2 ms
- Access Times: 150 ns, 200 ns, 250 ns
- Low power: 528 mW max
- TTL compatible: all inputs and output
- Gated \overline{CAS} —noncritical timing
- Read, Write, Read-Modify-Write and RAS-only Refresh cycles
- Page mode operation
- Industry standard 16-pin configuration

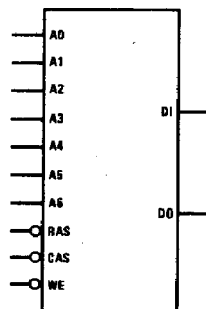
Block Diagram



Connection Diagram



Logic Diagram



Pin Names

- RAS Row Address Strobe
- CAS Column Address Strobe
- WE Write Enable
- A0–A6 Address Inputs
- DI Data Input
- DO Data Output
- VDD Power (12V)
- VCC Power (5V)
- VSS Ground
- VBB Power (-5V)

Order Number MM5298AJ-2, MM5298BJ-2,
MM5298AJ-3, MM5298BJ-3,
MM5298AJ-4 or MM5298BJ-4
See NS Package J16A

Order Number MM5298AN-2, MM5298BN-2,
MM5298AN-3, MM5298BN-3,
MM5298AN-4 or MM5298BN-4
See NS Package N16A

* For MM5298A A5 must be at V_{IL} during t_{RAH} .
For MM5298B A5 must be at V_{IH} during t_{RAH} .
** See the MST™ Program page 3.

Absolute Maximum Ratings (Note 1)

| | |
|--|-----------------|
| Storage Temperature | -65°C to +150°C |
| Power Dissipation | 1W |
| Voltage on Any Pin Relative to V _{BB} | -0.3V to +20V |
| (V _{SS} - V _{BB} ≥ 4.5V) | |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

Recommended DC Operating Conditions

| SYMBOL | PARAMETER | MIN | MAX | UNITS | NOTES |
|------------------|--|------|------|-------|-------|
| T _A | Ambient Temperature | 0 | 70 | °C | |
| V _{DD} | Supply Voltages | 10.8 | 13.2 | V | 2, 3 |
| V _{CC} | | 4.5 | 5.5 | V | 2, 3 |
| V _{SS} | | 0 | 0 | V | 2, 3 |
| V _{BB} | | -4.5 | -5.5 | V | 2, 3 |
| V _{IHC} | Input High Voltage, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ | 2.7 | 7.0 | V | 2 |
| V _{IH} | Input High Voltage, A0-A6, DI | 2.4 | 7.0 | V | 2 |
| V _{IL} | Input Low Voltage, All Inputs | -1.0 | 0.8 | V | 2 |

DC Electrical Characteristics Over the range of Recommended DC Operating Conditions unless otherwise noted

| SYMBOL | PARAMETER | MIN | MAX | UNITS | NOTES |
|-------------------|--|--|-----|-------|-------|
| I _{DD1} | Operating Current Average Power Supply Operating Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling; t _{RC} = t _{RC MIN}) | | 40 | mA | 4 |
| I _{CC1} | | | 200 | μA | 5 |
| I _{BB1} | | | | | |
| I _{DD2} | Standby Current Power Supply Standby Current ($\overline{\text{RAS}}$ = V _{IHC} , DO = High Impedance) | | 1.5 | mA | |
| I _{CC2} | | -10 | 10 | μA | |
| I _{BB2} | | | 100 | μA | |
| I _{DD3} | Refresh Current Average Power Supply Current, Refresh Mode ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}}$ = V _{IHC} ; t _{RC} = t _{RC MIN}) | | 30 | mA | 4 |
| I _{CC3} | | -10 | 10 | μA | |
| I _{BB3} | | | 200 | μA | |
| I _{DD4} | Page Mode Current Average Power Supply Current, Page Mode ($\overline{\text{RAS}}$ = V _{IL} , $\overline{\text{CAS}}$ Cycling; t _{PC} = 225 ns) | | 32 | mA | 4 |
| I _{CC4} | | | 200 | μA | 5 |
| I _{BB4} | | | | | |
| I _{I(L)} | Input Leakage Input Leakage Current, Any Input (V _{BB} = -5V, 0V ≤ V _{IN} ≤ 7V, All Other Pins not Under Test = 0V) | -10 | 10 | μA | |
| I _{O(L)} | Output Leakage Output Leakage Current (DO is Disabled, 0V ≤ V _{OUT} ≤ 5.5V) | -10 | 10 | μA | |
| V _{OH} | Output Levels Output High Voltage (I _{OUT} = -5 mA) | 2.4 | | V | |
| V _{OL} | | Output Low Voltage (I _{OUT} = 4.2 mA) | | 0.4 | V |

CAPACITANCE

| SYMBOL | PARAMETER | MIN | MAX | UNITS | NOTES |
|----------------|--|-----|-----|-------|-------|
| C _I | Input Capacitance A0-A6, DI | | 5 | pF | 6 |
| C _C | Input Capacitance $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ | | 10 | pF | 6 |
| C _O | Output Capacitance, DO | | 7 | pF | 6 |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}. When applying voltages to the device, V_{DD}, V_{CC} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Several cycles are required after power-up before proper device operation is achieved. Any 8 RAS cycles are adequate for this purpose.

Note 4: I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.

Note 5: I_{CC} depends on output load.

Note 6: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation C = IΔt/ΔV. Capacitance is guaranteed by periodic testing.

AC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted

| SYMBOL | PARAMETER | MM5298-2A, MM5298-2B | | MM5298-3A, MM5298-3B | | MM5298-4A, MM5298-4B | | UNITS | NOTES |
|------------------|---|-------------------------|--------|-------------------------|--------|-------------------------|--------|-------|--------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t _{RC} | Random Read or Write Cycle Time | 375 | | 375 | | 410 | | ns | 7, 8 |
| t _{RWC} | Read-Write Cycle Time | 375 | | 375 | | 515 | | ns | 7, 8 |
| t _{PC} | Page Mode Cycle Time | 170 | | 225 | | 275 | | ns | |
| t _{RAC} | Access Time from $\overline{\text{RAS}}$ | | 150 | | 200 | | 250 | ns | 9, 11 |
| t _{CAC} | Access Time from $\overline{\text{CAS}}$ | | 100 | | 135 | | 165 | ns | 10, 11 |
| t _{OFF} | Output Buffer Turn-Off Delay | 0 | 40 | 0 | 50 | 0 | 60 | ns | 12 |
| t _T | Transition Time (Rise and Fall) | 3 | 35 | 3 | 50 | 3 | 50 | ns | |
| t _{RP} | $\overline{\text{RAS}}$ Precharge Time | 100 | | 120 | | 150 | | ns | |
| t _{RAS} | $\overline{\text{RAS}}$ Pulse Width | 150 | 10,000 | 200 | 10,000 | 250 | 10,000 | ns | |
| t _{RSH} | $\overline{\text{RAS}}$ Hold Time | 100 | | 135 | | 165 | | ns | |
| t _{CAS} | $\overline{\text{CAS}}$ Pulse Width | 100 | 10,000 | 135 | 10,000 | 165 | 10,000 | ns | |
| t _{RCD} | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time | 20 | 50 | 25 | 65 | 35 | 85 | ns | 9 |
| t _{CRP} | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | -20 | | -20 | | -20 | | ns | |
| t _{ASR} | Row Address Set-Up Time | 0 | | 0 | | 0 | | ns | |
| t _{RAH} | Row Address Hold Time | 20 | | 25 | | 35 | | ns | |
| t _{ASC} | Column Address Set-Up Time | -10 | | -10 | | -10 | | ns | |
| t _{CAH} | Column Address Hold Time | 45 | | 55 | | 75 | | ns | |
| t _{AR} | Column Address Hold Time Referenced to $\overline{\text{RAS}}$ | 95 | | 120 | | 160 | | ns | |
| t _{RCS} | Read Command Set-Up Time | 0 | | 0 | | 0 | | ns | |
| t _{RCH} | Read Command Hold Time | 0 | | 0 | | 0 | | ns | |
| t _{WCH} | Write Command Hold Time | 45 | | 55 | | 75 | | ns | |
| t _{WCR} | Write Command Hold Time Referenced to $\overline{\text{RAS}}$ | 95 | | 120 | | 160 | | ns | |
| t _{WP} | Write Command Pulse Width | 45 | | 55 | | 75 | | ns | |
| t _{RWL} | Write Command to $\overline{\text{RAS}}$ Lead Time | 60 | | 80 | | 100 | | ns | |
| t _{CWL} | Write Command to $\overline{\text{CAS}}$ Lead Time | 60 | | 80 | | 100 | | ns | |
| t _{DS} | Data-In Set-Up Time | 0 | | 0 | | 0 | | ns | 13, 14 |
| t _{DH} | Data-In Hold Time | 45 | | 55 | | 75 | | ns | 13, 14 |
| t _{DHR} | Data-In Hold Time Referenced to $\overline{\text{RAS}}$ | 95 | | 120 | | 160 | | ns | |
| t _{CP} | $\overline{\text{CAS}}$ Precharge Time (for Page Mode Cycle Only) | 60 | | 80 | | 100 | | ns | |
| t _{REF} | Refresh Period | | 2 | | 2 | | 2 | ms | |
| t _{WCS} | $\overline{\text{WE}}$ to $\overline{\text{CAS}}$ Set-Up Time | -40 | | -40 | | -40 | | ns | 14 |
| t _{CWD} | $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay | 70 | | 95 | | 125 | | ns | 15 |
| t _{RWD} | $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay | 120 | | 160 | | 200 | | ns | 15 |

Note 7: The specifications for t_{RC}(MIN) and t_{RWC}(MIN) are used only to indicate cycle time at which proper operation over the full temperature range is guaranteed.

Note 8: Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Timing measurements are made between V_{IHC}(MIN) or V_{IH}(MIN) and V_{IL}(MAX), and assume t_T = 5 ns.

Note 9: Assumes row-limited access, i.e., t_{RCD} ≤ t_{RCD}(MAX). If this condition is not satisfied, then note 10 applies.

Note 10: Assumes column-limited access, i.e., t_{RCD} > t_{RCD}(MAX).

Note 11: Equivalent load is 2 standard TTL inputs plus 100 pF.

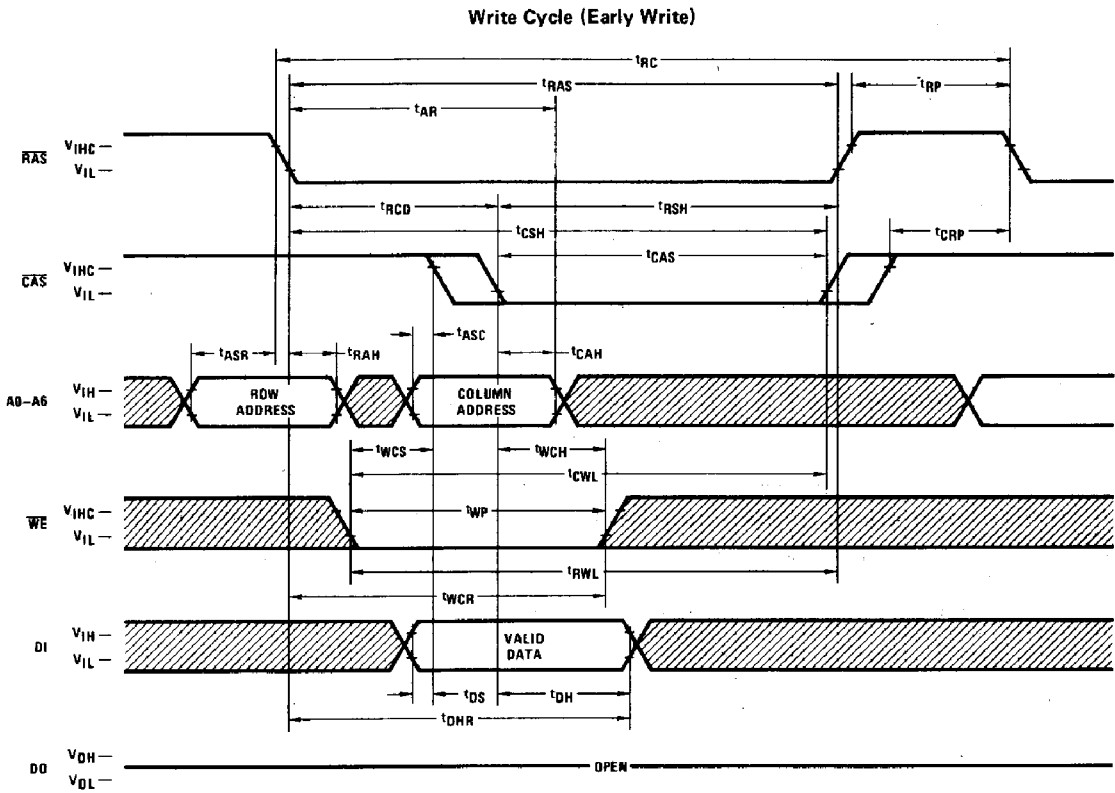
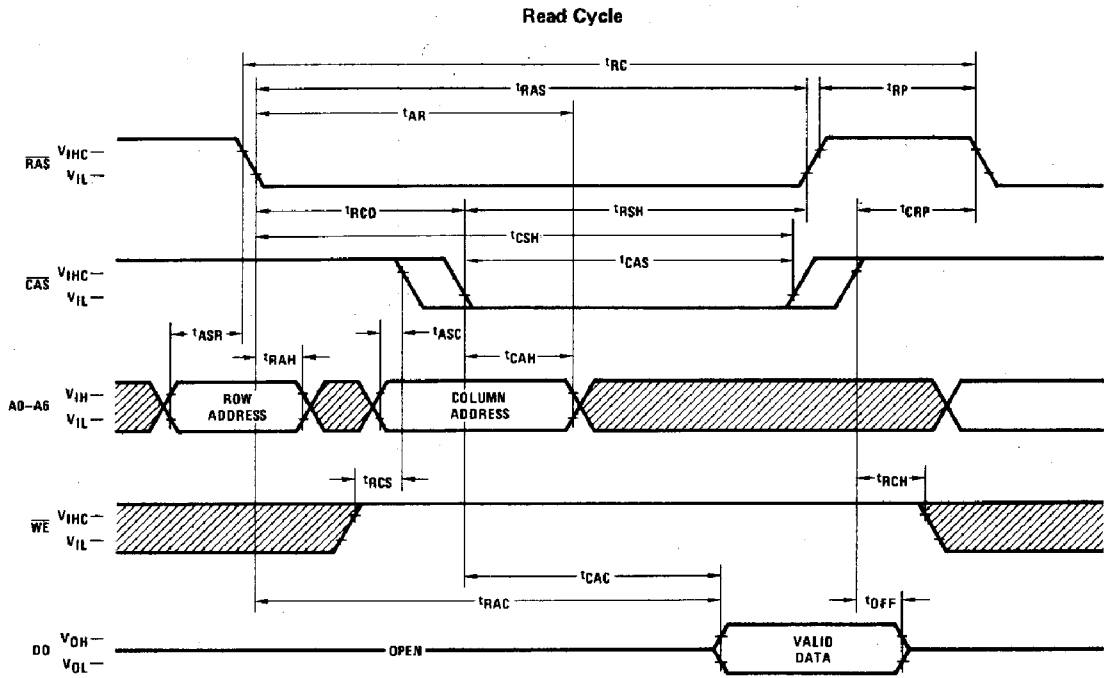
Note 12: $\overline{\text{CAS}}$ going high disables the Data Output. t_{OFF} is the delay to the high impedance state.

Note 13: These parameters are referenced to the negative edge of $\overline{\text{CAS}}$ in an early-write cycle and to the negative edge of $\overline{\text{WE}}$ in a Read-Modify-Write cycle. (See Note 14 below).

Note 14: If t_{WCS} ≥ t_{WCS}(MIN), the Data Output is guaranteed to remain in the high impedance state for the duration of the cycle. This is the "early-write" cycle.

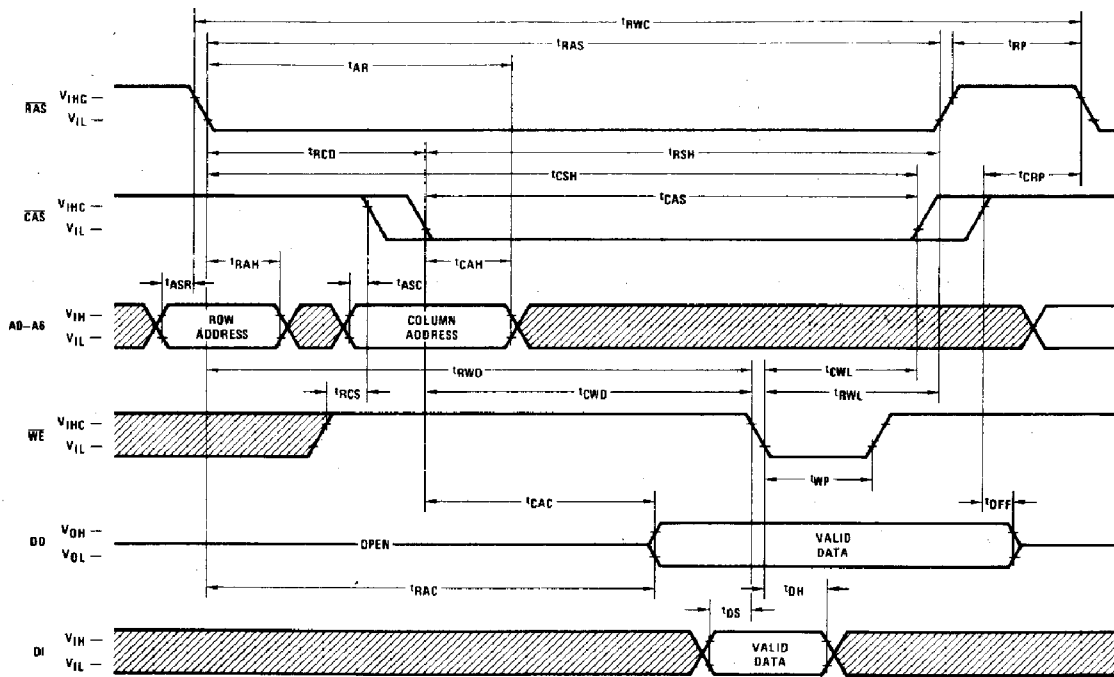
Note 15: If t_{CWD} ≥ t_{CWD}(MIN) and t_{RWD} ≥ t_{RWD}(MIN), the Data Output will contain the original data in the selected cell. This is the Read-Modify-Write cycle. If either of these conditions is not satisfied, the output will be indeterminate unless the early-write condition of Note 12 is met.

Switching Time Waveforms

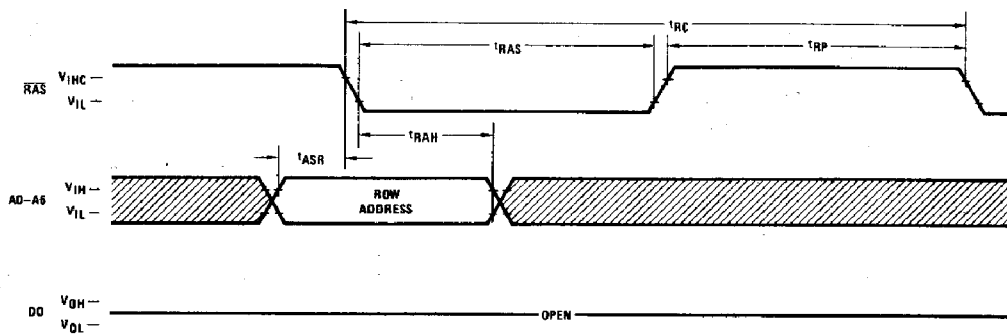


Switching Time Waveforms (Continued)

Read-Write Cycle, Read-Modify-Write Cycle



RAS-Only Refresh Cycle

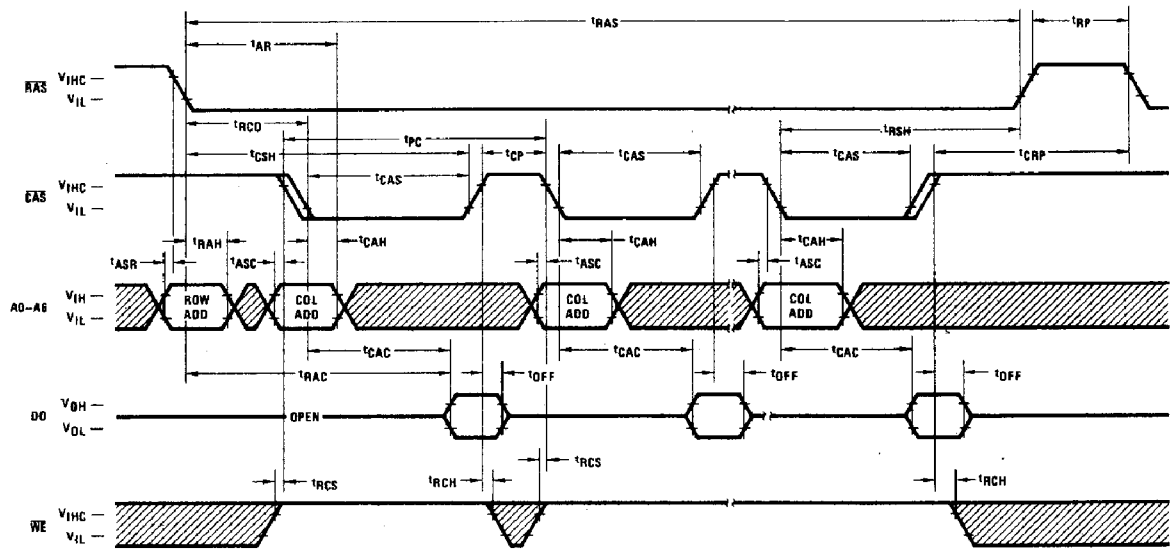


Note. $\overline{\text{CAS}} = V_{IH}$. $\overline{\text{WE}} = \text{don't care}$

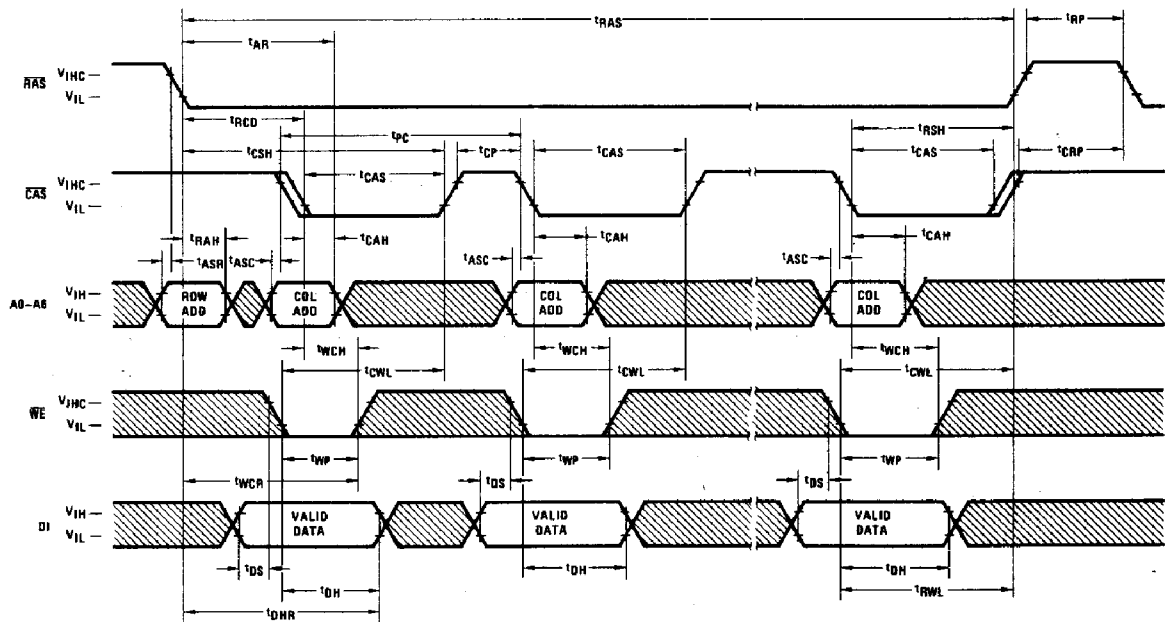
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Switching Time Waveforms (Continued)

Page Mode Read Cycle



Page Mode Write Cycle



Note. Standard part not tested for page mode