



CLKOUT is 8MHz

Open Collector
 Must be left in high state when inactive

Wait out gates an 8MHz clock to the Z80 Wait logic which retriggers an RC wait pulse to the processor every time it sees a falling edge on this line. This is necessary because bus WAIT is not connected to the Z80, but rather to a retriggerable (falling edge) one-shot that generates the Z80 WAIT signal on the Digital Group Z80 CPU card. Wait is approx 35uS for simple requests.

