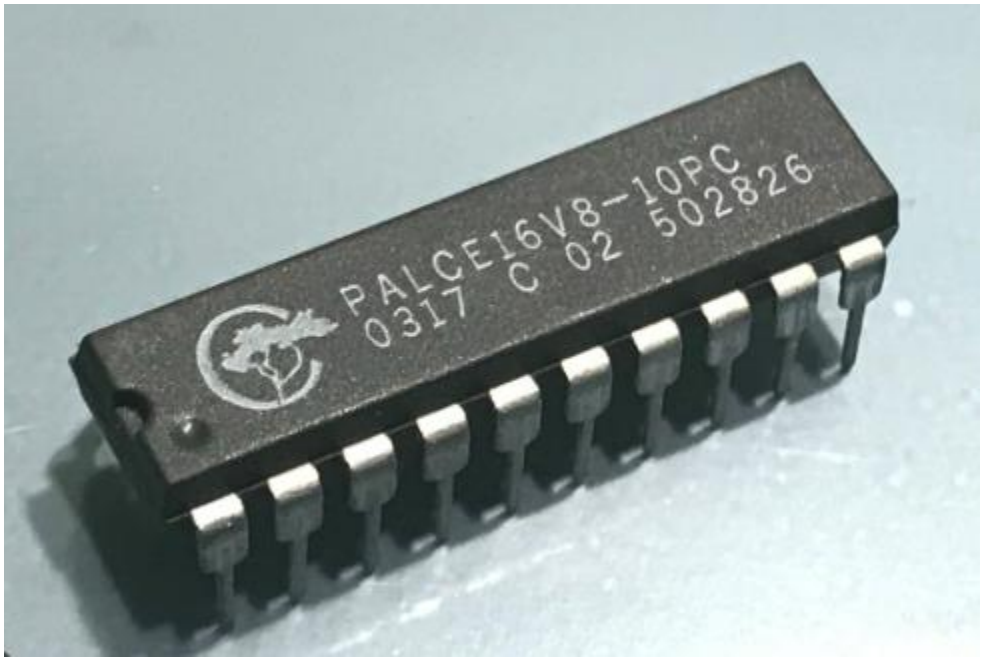
# PAL Tools




It is hard to find tools that still work on the now obsolete PAL chips of the ‘90s. This document describes one such tool that you can use and how to get it to work on Win10.

## Contents

# Download

Download the tool from the following link:

https://www.microchip.com/en-us/products/fpgas-and-plds/spld-cplds/pld-design-resources

**Serial Number for WinCUPL: 60008009**

Download the CUPL language documentation here:

https://ece-classes.usc.edu/ee459/library/documents/CUPL_Reference.pdf

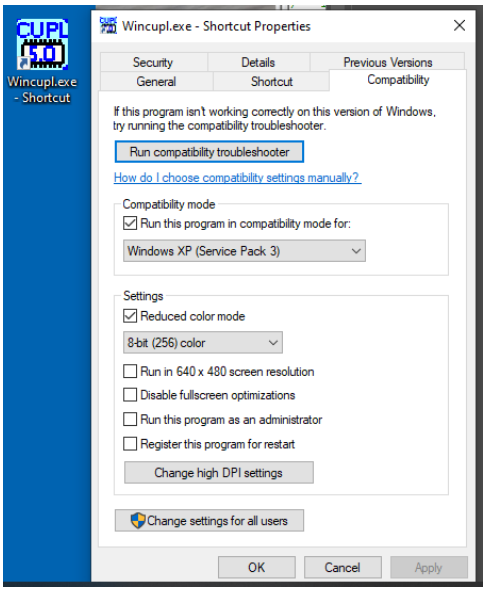
# Install

Run the installer downloaded in the previous step.

Choose whatever directory you want – keep in mind that it will create a folder structure inside this folder that contains “WinCupl” so if you name your install folder “WinCupl” it gets a little confusing.

# Setup

Create a desktop shortcut to “Wincupl.exe” with the following compatibility:



## Fix DLL Issues

When you then double-click on the shortcut, you are very likely to get a bunch of warnings about missing DLL files. Here are the steps to resolve them:

1. Open an admin command prompt
2. Run “cd c:\windows\SysWOW64”
3. Run “regsvr32 /u xxxxxx32.ocx”
4. Run “regsvr32 /I xxxxxx32.ocx”

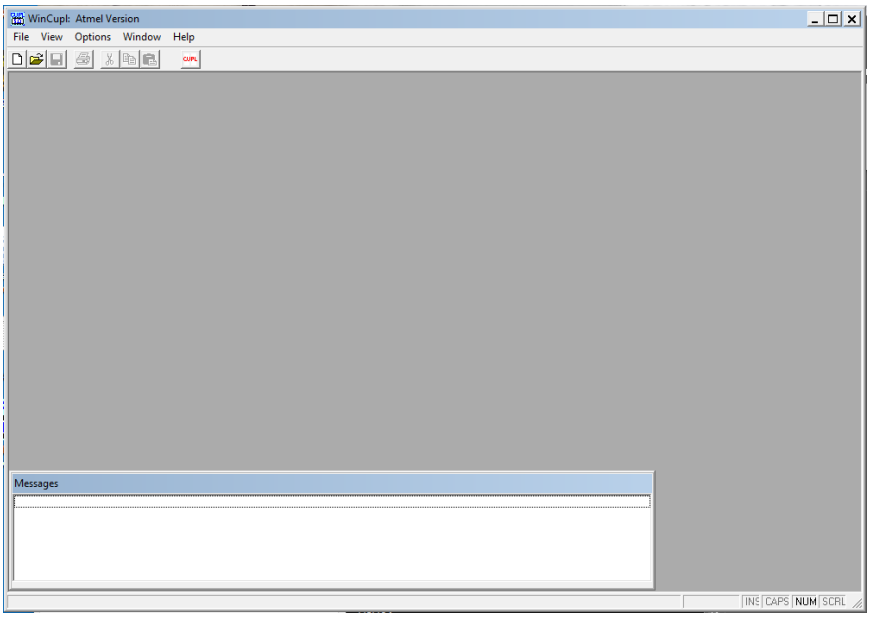
You will also get a warning every time that the entry point “DLLInstall” could not be found – just ignore this.

You MUST do step 3 (uninstall) before step 4 (install) don’t skip this.

I had to do this for the following files (your list may be different. Just keep doing this for every file it complains about until the program starts running.)

- Comdlg32.ocx
- Dwsbc32.ocx
- RICHTX32.ocx
- TABCTL32.ocx

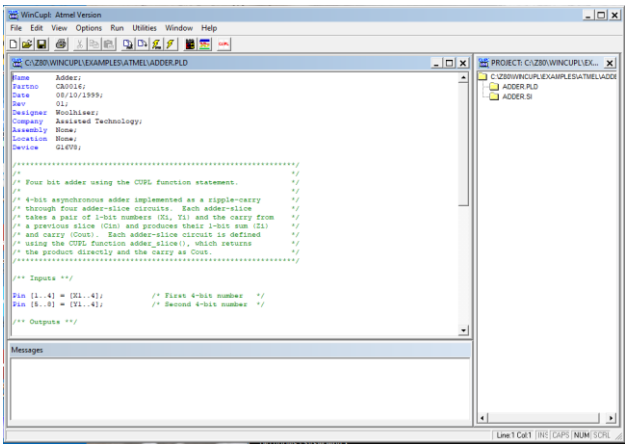
Once you resolve all the missing DLL issues you should see something like the following. You should now be ready to start using the tool.



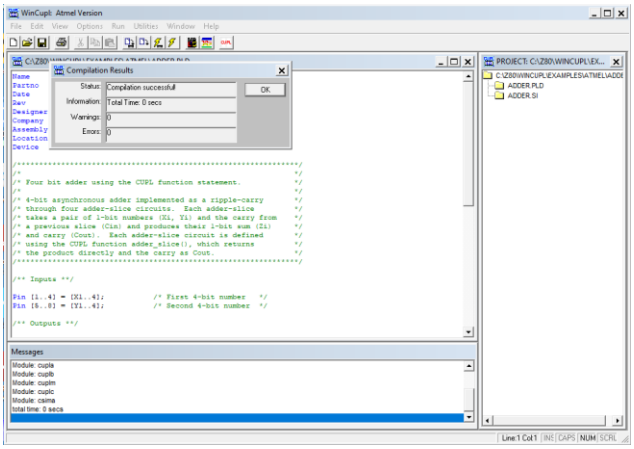
# Basic Tool Operation

Here was a helpful forum discussion: http://forum.6502.org/viewtopic.php?f=10&t=7147

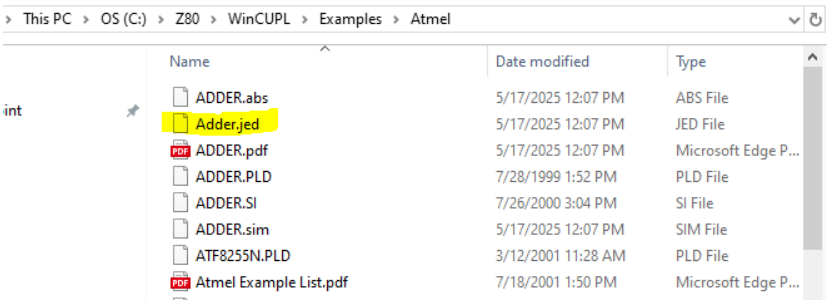
Use the Examples folder as a guide to how to create your PLD file.



Press F9 (device dependent compile)



If you have no errors, you will then see a generated JEDEC file in the same folder as your PLD file. You can now use this to burn your PLD using an appropriate device programmer.



# Running Command Line Tools

WinCUPL is basically just a GUI front end to a set of DOS command line tools

You can use the command line tools when the GUI fails or for easier integration into make files.

Running “cupl.exe” can be accomplished these commands (replace paths with your install paths):

- set LIBCUPL=c:\Z80\WinCUPL\Shared\cupl.dl
- c:\Z80\WinCUPL\Shared\cupl.exe -jaxfl p16r4 16R4_Test.PLD

You (according to the documentation) should be able to specify the target device in the command line (the P16R4) above, but it causes the build to continually fail. Removing the ‘p16r4’ target option allows the tool to compile without errors.

Usage: cupl -flags <library.dl> <device> file
Where: flags
Download file formats
-j JEDEC output (jedec compatible programming file)
-h ASCII-hex output (PROM ASCII hex download file)
-i HL output (Signetics IFL devices only)
-n download filename=PLD filename
Output file formats
-a absolute file (required for simulation)
-l listing file (generate error listing file)
-e expanded macro definition file (macros and REPEAT statements)
-x expanded product terms (generate documentation file)
-f fuse plot/chip diagram (attach fuse plot in documentation file)
-b Berkeley PLA file (generate a Berkeley PLA file for fitters)
-o One-hot-bit state machine (use one-hot bit encoding for state machines)
-d Deactivate unused OR terms (remove unused product terms in IFL devices)
-r Disable product term merging (identical p-term generation in IFL devices)
-g Program security fuse (blow security fuse after programming if supported)
-u Use specified library, must immediately precede library name (override library specified in the environment)
-s Simulate after compile (simulate after successful compilation)
Optimization methods
-kb Optimize product term usage (overrides the DEMORGAN statement in file)
-kd Demorganize all pins and pinnodes (overrides the DEMORGAN statement)
-ks Force product term sharing (enable group reduction)
-kx Do not expand XOR equations (virtual or fitter that supports XOR gates)
Minimization Method
-m0 No minimization (no logic reduction)
-m1 Quick minimization (default. Lowest memory usage and fastest)
-m2 Quine-McCluskey minimization (highest memory usage and slowest.)
-m3 Presto minimization (good trade-off between memory and speed)
-m4 Espresso minimization (high memory usage and slow. Good for fitter designs)

## Unable to Target PAL16R4 Issue

Specifying the following allows CUPL to compile. But every time I try to specify 16R4 or any variant – even those I can see in the device binary file such as “p16r4a” – the tools abort with target not found in library.

```
Device      g16v8;    /* g16v8 works, but 16r4 does not */
```

I have not figured out how to get around this yet.